

UNIVERSITA' DEGLI STUDI DI GENOVA
AREA RICERCA, TRASFERIMENTO TECNOLOGICO E TERZA MISSIONE
SERVIZIO RICERCA
SETTORE RICERCA NAZIONALE

IL RETTORE

- Visto il Decreto Rettoriale n. 2059 del 16/05/2025, parzialmente rettificato con Decreto Rettoriale n. 2220 del 27/05/2025, con il quale è stato indetto il concorso per titoli e colloquio, per il conferimento di 5 borse di ricerca post-lauream, di tipo starting, della durata di 6 mesi, dell'importo di euro 6.464,28 (seimilaquattrocentosessantaquattro/28) cadasuna, eventualmente rinnovabili, per lo svolgimento di una ricerca sul tema: "Progettazione (schematic-to-GDS) di celle analogiche con ampio utilizzo di celle digitali finalizzato all'aumento dell'automatizzazione del flusso di progetto", presso il Dipartimento DITEN dell'Università degli Studi di Genova;
- Visto il Decreto Rettoriale n. 2448 del 10/06/2025 con il quale è stata costituita la Commissione giudicatrice per il conferimento della suddetta borsa di ricerca;
- Visto il verbale della Commissione giudicatrice del concorso in parola, riunitasi in data 16/06/2025;
- Constatata la regolarità della procedura seguita;

DECRETA

Art. 1

Sono approvati gli atti del concorso di cui in premessa e la seguente graduatoria di merito:

1. Tommaso Troccoli	punti 80/100;
2. Marco Vercellino	punti 76/100;
3. Lorenzo Iezzi	punti 72/100;
4. Giuseppe Contarino	punti 71/100;
5. Davide Pangallo	punti 71/100.

Gli altri candidati non raggiungono il punteggio minimo ai fini dell'idoneità alla fruizione della borsa. Sotto condizione dell'accertamento dei requisiti di cui al bando, sono dichiarati vincitori del concorso in parola il Dott. Tommaso Troccoli, il Dott. Marco Vercellino, il Dott. Lorenzo Iezzi, il Dott. Giuseppe Contarino, il Dott. Davide Pangallo.

Genova,

IL RETTORE
(firmato digitalmente)



Giuseppe Contarino



● PRESENTAZIONE

Sono uno **studente** magistrale di **Ingegneria Elettronica** presso la Scuola Politecnica dell'Università degli Studi di Genova.

Durante i miei anni di studio ritengo di aver ottenuto un solido background tecnico con un forte interesse sulla Microelettronica Analogica.

Se mi dovessi descrivere in tre aggettivi di certo utilizzerai: **Concreto, pragmatico e affidabile**
inserire una tua descrizione...

● PROGETTI

01/03/2024 – 15/06/2024

Two-stage OTA: Design flow and Specs analysis

Il progetto prevedeva la realizzazione di un amplificatore operazionale a due stadi: **uno stadio differenziale** seguito da **uno stadio in classe B**. Nella fase finale è stata effettuata la verifica delle specifiche. È stato utilizzato Cadence Virtuoso per la progettazione.

01/09/2024 – 21/12/2024

Design of a Ring Oscillator and Tapered Buffer to drive a load of 25pF

Il progetto prevedeva la realizzazione di un **ring oscillator** e di un **tapered buffer** per pilotare un carico da **35 pF**, con verifica finale delle specifiche. Sono stati utilizzati i tool open-source XSchem e Magic per progettazione e layout.

● ISTRUZIONE E FORMAZIONE

01/09/2024 – ATTUALE Genova, Italia

LAUREA MAGISTRALE IN INGEGNERIA ELETTRONICA

 Università degli Studi di Genova

Sito Internet www.unige.it | **Livello EQF** Livello 7 EQF

01/09/2019 – 13/06/2023 Genova, Italia

LAUREA TRIENNALE IN INGEGNERIA BIOMEDICA

 Università degli Studi di Genova

Sito Internet www.unige.it | **Livello EQF** Livello 6 EQF

15/09/2014 – 03/07/2019 Giarre, Italia

DIPLOMA LICEO CLASSICO M. Amari

Sito Internet <https://www.iisamari.edu.it/> | **Livello EQF** Livello 5 EQF

● CONFERENZE E SEMINARI

06/05/2025 – 08/05/2025 Didcot, STFC, RAL

Introduction to Digital Mixed Signal IC Design

L'obiettivo del corso è fornire la teoria e il flusso di progettazione per un progetto digitale a segnali misti dominati in un tipico processo CMOS. Il corso coprirà le fasi principali del flusso e gli strumenti corrispondenti, con il supporto di

lezioni ed esercitazioni pratiche. Il corso copre la metodologia di progettazione, la simulazione a segnale misto, l'astrazione analogica e l'implementazione digitale-mista.

La teoria e i concetti fondamentali vengono introdotti attraverso le lezioni e dimostrati con esercitazioni pratiche utilizzando gli strumenti Cadence del portafoglio EUROPRACTICE, con un esempio di progetto implementato nel processo CMOS UMC a 65 nm.

26/08/2024 – 30/08/2024 Leuven, Belgio

ASIC design introduction: From concept to silicon

Questa summer school copre in modo esaustivo diversi aspetti ed è suddivisa in vari argomenti dettagliati, tra cui teoria e concetti. Al termine di questa scuola estiva, i partecipanti avranno una comprensione generale del flusso di progettazione ASIC.

Autorizzo il trattamento dei miei dati personali presenti nel CV ai sensi dell'art. 13 d. lgs. 30 giugno 2003 n. 196 - "Codice in materia di protezione dei dati personali" e dell'art. 13 GDPR 679/16 - "Regolamento europeo sulla protezione dei dati personali".



Lorenzo lezzi

ABOUT MYSELF

Bachelor's graduate in Electronic Engineering and Information Technologies at the University of Genoa, currently pursuing a Master's degree in Electronic Engineering. I am seeking a position in the electronics field that will allow me to further develop the theoretical and practical skills acquired during my studies.

EDUCATION AND TRAINING

Master's Degree in Electronic Engineering

[03/2024 – Current]

City: Genoa | Country: Italy

Bachelor's Degree in Electronic Engineering and Information Technologies

[09/2019 – 02/2024]

City: Genoa | Country: Italy

Technical Diploma in Electronics and Telecommunications

[09/2014 – 06/2019]

City: Sanremo | Country: Italy

SKILLS

Software

Arduino IDE / Matlab / LTSpice and PSpice / Cadence

Programming Languages

C++ / C

PROJECTS

Autonomous docking of a rover using infrared sensors

Implementation of two different infrared-based sensing technologies, aimed at enabling a semi-autonomous rover, designed and built at the SEA Lab of UniGe, to approach a ground station. The rover/base pair is fully functional and effective in any environment.

Colpitts oscillator

Designed with an oscillation frequency of 8 MHz and implemented entirely in software using LTSpice

Frequency synthesizer based on PLL (Phase-Locked Loop)

built on breadboard and FPGA, with experimental validation

Two-stage OTA

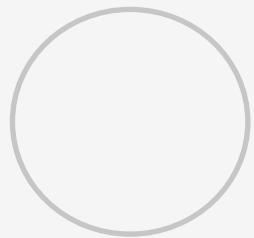
Design flow and specs analysis on Cadence

Schmitt trigger

Design flow, specs analysis and layout on Cadence for four different configurations



Davide Pangallo



● ABOUT MYSELF

Recent graduate in Electronic Engineering from the University of Genoa, motivated to contribute to technological innovation. Naturally collaborative, with good communication skills and a team-oriented approach.

● EDUCATION AND TRAINING

02/2024 – CURRENT Genova, Italy

MASTER'S DEGREE IN ELECTRONIC ENGINEERING

Level in EQF EQF level 7

09/2019 – 02/2024 Genova, Italy

BACHELOR'S DEGREE IN ELECTRONIC ENGINEERING AND INFORMATION TECHNOLOGIES

Level in EQF EQF level 6

09/2014 – 06/2019 Sanremo, Italy

TECHNICAL DIPLOMA IN ELECTRONICS AND TELECOMMUNICATIONS

● WORK EXPERIENCE

LEONARDO S.P.A – GENOVA, ITALY

ELECTRONICS ENGINEERING TECHNICIAN – 03/09/2024 – 06/03/2025

Conducted a project in the embedded systems field using VHDL. Supported the study of electrical schematics and PCBs already developed for industrial equipment, performing lab tests on the bench for analysis and optimization of critical sections such as DC-DC converters. This experience also allowed me to understand corporate dynamics and the interaction between teams and departments in completing complex projects.

● LANGUAGE SKILLS

Mother tongue(s): **ITALIAN**

Other language(s):

	UNDERSTANDING		SPEAKING		WRITING
	Listening	Reading	Spoken production	Spoken interaction	
ENGLISH	B2	B2	B2	B2	B2
FRENCH	A1	A1			

Levels: A1 and A2: Basic user - B1 and B2: Independent user - C1 and C2: Proficient user

● PROJECTS

RF Oscillator on PCB: designed in LTSpice and realized in KiCad.

Frequency Synthesizer with PLL: implemented on FPGA and breadboard.

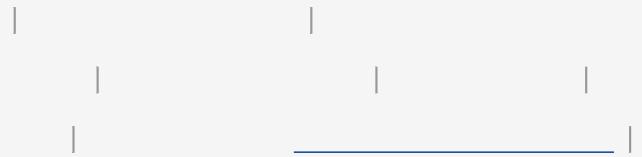
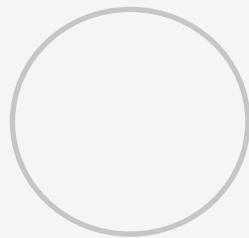
Wireless sensor network for indoor air quality monitoring: bachelor thesis with STM32WL55JC1 and Spec Sensors ULP5M-IAQ sensor.

Two-stage OTA Amplifier: design and verification in Cadence Virtuoso with 180nm CMOS technology.

Astable Multivibrators: schematic design and layout in Cadence Virtuoso.



Tommaso Troccoli



EDUCATION AND TRAINING

19/09/2023 – CURRENT Genova, Italy

MASTER'S DEGREE IN ELECTRONIC ENGINEERING University of Genoa

Website <https://corsi.unige.it/corsi/8732> | **Level in EQF** EQF level 7

19/09/2020 – 14/02/2024 Genova, Italy

BACHELOR'S DEGREE IN ELECTRONIC ENGINEERING AND INFORMATION TECHNOLOGIES University of Genoa

Website <https://corsi.unige.it/corsi/9273> | **Level in EQF** EQF level 6

19/09/2015 – 06/06/2020 Genova, Italy

HIGH SCHOOL DIPLOMA Liceo Statale Leonardo Da Vinci

Website <https://www.liceoleodavincige.edu.it/> | **Level in EQF** EQF level 4

CONFERENCES AND SEMINARS

06/05/2025 – 08/05/2025 Didcot

Introduction to Digital Mixed Signal IC Design

The course objective is to provide the theory and design flow for a mixed-signal dominated digital project in a typical CMOS process. The course will cover the main stages of the design flow and the corresponding tools, supported by lectures and practical exercises. It addresses design methodology, mixed-signal simulation, analog abstraction, and mixed-signal implementation.

Fundamental theory and concepts are introduced through lectures and demonstrated with practical exercises using Cadence tools from the EUROPRACTICE portfolio, with a sample project implemented in the 65 nm UMC CMOS process.

PROJECTS

06/03/2025 – 20/05/2025

1 GHz Colpitts oscillator

Design and simulation of a 1 GHz Colpitts oscillator, followed by PCB implementation and performance verification.

06/12/2024 – 06/02/2025

Patch Antenna Array

Design of a patch antenna array optimized to operate at 2.4 GHz, including analysis of radiation characteristics for wireless applications.

06/06/2024 – 06/10/2024

Two-stage Operational Amplifier

Design and implementation of a two-stage operational amplifier with differential input and class AB output, capable of driving both resistive and capacitive loads.

● SKILLS

Cadence | Ansys | STM32 | Vivado | Quartus | Python | Machine Learning | VHDL | C | Magic | Xschem | VS Code | LaTeX | Linux | Git | Microsoft Office | MATLAB | Arduino

● LANGUAGE SKILLS

Mother tongue(s): **ITALIAN**

Other language(s):

	UNDERSTANDING		SPEAKING		WRITING
	Listening	Reading	Spoken production	Spoken interaction	
ENGLISH	B2	B2	B2	B2	B2

Levels: A1 and A2: Basic user; B1 and B2: Independent user; C1 and C2: Proficient user

● DRIVING LICENCE

Driving Licence: AM

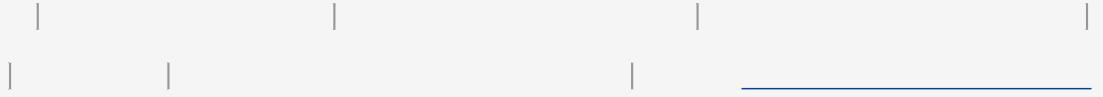
Driving Licence: A1

Driving Licence: A2

Driving Licence: B



Marco Vercellino



● ABOUT MYSELF

Bachelor's graduate in Electronic Engineering and Information Technologies from the University of Genoa, currently pursuing a Master's degree in Electronic Engineering. Motivated and detail-oriented, with a solid foundation in electronics, control systems, and digital technologies, and a strong interest in advanced applications and innovation in the field..

● WORK EXPERIENCE



TUTOR

One-on-one tutoring for STEM subjects Sept 2020– Present

Football Coach (age group 2007 to 2015) March 2021– August 2024

● EDUCATION AND TRAINING

01/09/2020 – 15/09/2023 Genova, Italy

BACHELOR'S DEGREE ELECTRONIC ENGINEERING AND INFORMATION TECHNOLOGIES UniGe

Website <https://unige.it> | Level in EQF EQF level 6

01/09/2023 – CURRENT Genova, Italy

MASTER'S DEGREE ELECTRONIC ENGINEERING UniGe

Website <https://unige.it> | Level in EQF EQF level 7

01/09/2015 – 30/06/2020 Genova, Italy

HIGH SCHOOL DIPLOMA Martin Luther King high school

Website <https://www.liceoking.edu.it/> | Level in EQF EQF level 5

● LANGUAGE SKILLS

Mother tongue(s): **ITALIAN**

Other language(s):

	UNDERSTANDING		SPEAKING		WRITING
	Listening	Reading	Spoken production	Spoken interaction	
SPANISH	B2	B1	B1	B1	B1
ENGLISH	B2	B2	B2	B2	B2

Levels: A1 and A2: Basic user - B1 and B2: Independent user - C1 and C2: Proficient user

● PROJECTS

Colpitts Oscillator

Design and implementation exclusively at the software level on LTSpice. Frequency synthesizer based on PLL (Phase-Locked-Loop): implementation on breadboard and FPGA with experimental verification. Operating frequency: 9.5 MHz.
Tools Used: LTSpic

Ring Oscillator

Schematic design and layout, at a given frequency, using Magic and Xschem, based on the state of the art.
Tools Used: Magic, Xschem, NetGen

Custom Operational Amplifier

Design and simulation using Cadence of an OpAmp composed of a MOS differential pair and a Class AB output stage in BJT.

Tools Used: Cadence

Embedded system for data collection

End-to-end development of an embedded system for the collection and classification of sports data (using a machine learning algorithm), with a user interface.

Tools Used: Arduino Nano BLE Sense, Flutter, Arduino IDE

Tow-Thomas filter

Design, simulation, and layout of a Tow-Thomas filter with low-pass and band-pass outputs using operational amplifiers, based on the state of the art, carried out with Cadence.

Tools Used: Cadance

Self-balancing robot

Design and implementation of a two-wheeled self-balancing robot with PID controller.

Tools Used: C++, ESP32 board

Regenerative Braking ABS for BLDC motor

Design and simulation of a regenerative braking ABS system for a BLDC motor.

Tools Used: Simulink

DRIVING LICENCE

Driving Licence: A2

Driving Licence: B